

IN THE CLAIMS

1. (Previously presented) A semiconductor multi-chip package comprising:
a package substrate including a surface having a plurality of bonding tips formed thereon;
and
two or more semiconductor chips mounted on the substrate surface, the two or more semiconductor chips each including:
a semiconductor substrate having integrated circuits formed on a cell region and a peripheral circuit region adjacent to each other;
a bond pad-wiring pattern formed on the semiconductor substrate;
a pad-rearrangement pattern directly contacting the bond pad-wiring pattern, the pad-rearrangement pattern including bond pads disposed over at least a part of the cell region; and
an insulating layer formed on the pad-rearrangement pattern,
wherein the bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate,
wherein the bond pads included with the pad-rearrangement pattern are exposed through the insulating layer,
wherein each bonding tip is electrically connected to a corresponding one of the bond pads.
2. (Cancelled)
3. (Original) The multi-chip package of claim 1, wherein the two or more chips are vertically stacked.
4. (Original) The multi-chip package of claim 1, wherein the two or more chips comprise the same type of chips.
5. (Cancelled)
6. (Original) The multi-chip package of claim 1, wherein one of the two or more chips is a memory chip and the other chip is a non-memory chip.

7. (Original) The multi-chip package of claim 1, wherein one of the two or more chips is a DRAM and the other chip is a flash memory.

8. (Original) The multi-chip package of claim 1, wherein the bond pads are formed along sides of the semiconductor substrate.

9. (Original) The multi-chip package of claim 1, wherein a portion of the pad-rearrangement pattern extends substantially from the center region of the semiconductor substrate toward an edge of the semiconductor substrate.

10. (Previously presented) The multi-chip package of claim 1, wherein the bond pad-wiring pattern is formed on a portion of the peripheral circuit region and extends across a portion of the cell region.

11. (Original) The multi-chip package of claim 1, wherein the bond pad-wiring pattern is formed entirely within the peripheral circuit region.

12-23. (Cancelled)

24. (Previously presented) A multi-chip package comprising:
a first chip; and
a second chip formed over the first chip,
wherein the first chip includes:
a bond pad-wiring pattern formed substantially in a center region of the first chip;
a pad-rearrangement pattern directly contacting the bond pad-wiring pattern; and
an insulating layer formed on the pad-rearrangement pattern,
wherein the pad-rearrangement pattern includes a first bond pad disposed at an edge of the first chip,
wherein the first bond pad is exposed through the insulating layer.

25. (Previously presented) The multi-chip package of claim 24, wherein the pad-rearrangement pattern includes a second bond pad, and wherein the first and second bond pads are respectively disposed along opposing edges of the first chip.

26. (Previously presented) The multi-chip package of claim 25, wherein the pad-rearrangement pattern extends substantially from the center region of the first chip toward the edge of the first chip.

27. (Previously presented) The multi-chip package of claim 24, wherein the bond pad-wiring pattern is formed on a first surface of the first chip, and wherein the second chip is mounted on the first surface of the first chip.

28. (Previously presented) The multi-chip package of claim 27, further comprising a spacer interposed between the first chip and the second chip.

29. (Previously presented) The multi-chip package of claim 24, further comprising a substrate on which the first chip is mounted.

30. (Previously presented) The multi-chip package of claim 29, wherein the substrate comprises a printed circuit board, a tape wiring substrate or a lead frame.

31-32. (Cancelled)

33. (Previously presented) The multi-chip package of claim 24, wherein the first bond pad disposed at an edge of the first chip is also disposed to be under the second chip.

34. (Previously presented) The multi-chip package of claim 24, wherein the first and second chips comprise the same type of chips.

35. (Cancelled)

36. (Previously presented) A multi-chip package comprising:

a lower chip; and
an upper chip formed over the lower chip, wherein the upper chip includes:
an upper bond pad-wiring pattern formed substantially in a center region of the upper chip;
an upper pad-rearrangement pattern directly contacting the upper bond pad-wiring pattern; and
an upper insulating layer formed on the upper pad-rearrangement pattern, wherein the upper pad-rearrangement pattern includes a upper bond pad disposed at an edge of the upper chip, wherein the upper bond pad is exposed through the upper insulating layer.

37. (Previously presented) The multi-chip package of claim 36, wherein the lower chip includes:

a lower bond pad-wiring pattern formed substantially in a center region of the lower chip; and

a lower pad-rearrangement pattern electrically connected to the lower bond pad-wiring pattern, wherein the lower pad-rearrangement pattern includes a lower bond pad disposed at an edge of the lower chip.

38. (Previously presented) The multi-chip package of claim 37, wherein the lower bond pad-wiring pattern is formed on a first surface of the lower chip, and wherein the upper chip is mounted on the first surface of the lower chip.

39. (Cancelled)

40. (Previously presented) The multi-chip package of claim 36, further comprising a substrate on which the lower chip is mounted.

41. (Cancelled)

42. (Previously presented) The multi-chip package of claim 40, wherein the lower chip includes a center pad-type bond pad.

43-46. (Cancelled)

47. (Previously presented) A semiconductor multi-chip package comprising:
a first chip mounted on a package substrate; and
a second chip mounted on the first chip with a spacer disposed therebetween, wherein the first chip includes:
bond pad-wiring patterns formed substantially in a center region of the first chip;
pad-rearrangement patterns directly contacting the bond pad-wiring patterns; and
insulating layers formed on the pad-rearrangement patterns,
wherein the pad-rearrangement patterns include bond pads disposed along opposing edges of the first chip, wherein the spacer is placed between the bond pads,
wherein the bond pads included with the pad-rearrangement patterns are exposed through the insulating layers.

48. (Previously presented) The semiconductor multi-chip package of claim 47, wherein the spacer is disposed over the bond pad-wiring patterns formed substantially in a center region of the first chip.

49. (Previously presented) The semiconductor multi-chip package of claim 48, wherein each bonding tip is electrically connected to a corresponding one of the bond pads through a bonding wire.

50. (Currently amended) The semiconductor multi-chip package of claim 49, ~~wherein the two or more chips comprise at least a lower chip and an upper chip, the upper chip disposed over the lower chip, and~~ wherein the spacer provides a sufficient space between the ~~lower first chip~~ and the ~~upper second chip~~ for the bonding wire to connect the ~~lower first chip~~ with the package substrate.

51. (Previously presented) The semiconductor multi-chip package of claim 1, wherein the cell region comprises a memory cell array region.

52. (Cancelled)

53. (Cancelled)